David Eitan Lesman

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Education

Imperial College London — London, UK
MEng Electrical and Electronic Engineering — *Sep. 2024 – June 2028*

- **Relevant Modules**: Computer Architecture, Digital Design (SystemVerilog), Circuit Design, Signal Processing, Electromagnetism

Experience

Electrical Engineering Intern — Jun. 2026 – Sep. 2026
MATERIAL — *Miami, US*

- Designed and wired the electronics for v2 of the Material Hybrid printer with the Lead Printer Engineer: 6 motors across 3 axes, custom PCB, and Raspberry Pi–based motor feedback capture.
- Built laser cutting alignment software with trace outline preview and a fiducial-based auto-aligner (beta), reducing anode/cathode/pouch cutting time roughly 5x.
- Wrote printer firmware and operator control software: torque-sensing homing, toolhead calibration via Panasonic PM-K25 sensors, toolchanger control, and a gcode console.

Hardware Engineering Intern — Aug. 2025 – Sep. 2025
Splash — *Miami, US*

- Built the hardware and firmware for a Raspberry Pi + Neo-6M GPS tracker, taking a single-board prototype from concept to working demo in under 5 weeks.
- Developed a live dashboard for device location and status; used to demonstrate technical feasibility to prospective investors.

Co-Founder — April 2022 – Dec. 2023
helpukrainians.be — *Remote, BE*

- Designed and deployed a volunteer-run platform matching donation offers and requests across Belgium during the Ukraine crisis; kept online and in daily use for 20+ months with a 2-person team.

Software Engineering Fellow — July 2024 – Sep. 2024
Headstarter AI — *Remote, US*

- Shipped five full-stack projects in a 7-week fellowship using Django, JavaScript, and OpenAI/Gemini APIs, including Stripe payments and user authentication.

Projects

Smart Grid Energy Management System | *PID Control, MQTT, MATLAB* — May 2026 – Jun. 2026

- Owned the supercapacitor storage subsystem of a networked DC microgrid built by a 6-person team; implemented ramped PID current control holding tracking error under 0.3A within the 1A/1s datasheet limit.
- Characterised the 0.45F capacitor bank and raised the bus voltage from 12V to 13.5V, increasing usable storage from 30J to 40J; quantified 10J/250s holding losses and fed the model into the team's MILP scheduler.
- Co-built the live telemetry and cost-tracking UI, updated over MQTT from all four grid nodes.

F1 Start Light Reaction Tester | *SystemVerilog, Quartus, DE10-Lite* — Autumn Term 2025

- Designed a SystemVerilog FSM driving a five-stage start-light sequence, with a 14-bit LFSR generating a pseudo-random lights-out delay so the release point could not be anticipated between runs.
- Measured reaction time to 1ms resolution using a synchronous edge detector on the button input, with results decoded to the 7-segment displays.

Awards & Competitions

Citadel Europe Spring Terminal (2025): 6th of all European teams, Python algorithmic trading competition.
Optiver–Imperial Trading Academy (2025): Selected for an options market-making programme.

Skills & Interests

Languages & Tools: Python, C++, SystemVerilog, MATLAB, KiCad, Quartus, Fusion 360, Git, Linux, NumPy
Spoken Languages: English, French, Dutch, Hebrew, Yiddish
Interests: Chess, competitive SSBU, tournament-level Padel